## REMARKS

The present Amendment cancels claims 1-18 and adds new claims 19-23. Therefore, the present application has pending claims 19-23.

In the Office Action the Examiner objected to various informalities in claims 1 and 5 and rejected claims 1-6, 9, 11-14 and 16-18 under 35 USC §112, second paragraph. As indicated above, claims 1-18 were canceled. Therefore, the objection to the informalities in claims 1 and 5 and the rejection of claims 1-6, 9, 11-14 and 16-18 are rendered moot. Accordingly, reconsideration and withdrawal of the above noted objection and rejection of the claims is respectfully requested.

Claims 1-18 stand rejected under 35 USC §102(b) as being anticipated by Dewey (U.S. Patent No. 5,724,501). As indicated above, claims 1-18 were canceled. Therefore, this rejection is rendered moot. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

As indicated above, the present Amendment adds new claims 19-23. New claims 19-23 are directed to features of the present invention not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, the features of the present invention as now more clearly recited in clams 19-23 are not taught or suggested by Dewey.

The present invention is directed to a storage system having a plurality of clusters and a communication path which connects each of the clusters. According to the present invention, each cluster includes a disk controller and a plurality of disk drives. The disk controller of the cluster includes a disk interface which connects the disk drives, a cache memory and a control memory.

Unique according to the present invention is that when a first disk controller receives from a host computer a write request, which requests updating data for updating data stored in disk drives of a second disk controller, the first disk controller checks whether the updating data is stored in the cache memory of the second disk controller, and if the updating data is not stored in the cache memory of the second cluster, the first disk controller sends the write request to the second disk controller via the communication path.

Further, unique according to the present invention is that the second disk controller, in response to the write request from the first disk controller, reads the updating data from the disk drives of the second disk controller to the cache memory of the second disk controller via the disk interface of the second disk controller and updates the data based on the write request.

The above described features of the present invention now more clearly recited in the claims are not taught or suggested by any of the references of record particularly Dewey whether taken individually or in combination with each other.

Differences between the features of the present invention and Dewey were described in the Remarks of the July 10, 2003 Amendment. The contents of said Remarks are incorporated herein by reference.

As discussed in the July 10, 2003 Amendment, the Examiner alleges that Dewey teaches a method for allowing a host computer to access data from a first storage controller by using a request to a second storage controller which also has a cache memory. However, Dewey simply teaches a method for recovering data in a cache memory of a second storage controller by access to a cache memory of first

storage controller. The Examiner's attention is directed to col. 12, lines 35-38 and the Abstract of Dewey.

Dewey teaches that a disk controller controls disk drives using a single processor such as, for example, local processor 15 as illustrated in Fig. 1 thereof. Further, Dewey teaches in Figs. 6 and 7 a plurality of controller circuits 401 each of which is connected to the same plurality of disk drives 404, 406 and 408 via disk interfaces 410, 412 and 414. As taught by Dewey, when either one of the controller circuits 401, 401' fails, data which may have been held in the controller circuit 401 are transferred to the other controller circuit 401 via the memory interface 420, 420' and the single dump link 426. Dewey teaches that the random access memories (RAM) 422 and 424 of each controller circuit 401, 401' is used so as to buffer data which is to be transferred between the controller circuits 401, 401' via the single dump link 426.

Thus, as is quite clear from the teachings in Dewey, the single dump link 426 between the controller circuits 401 and 401' and the RAMs 422 and 424 are only used when one of the controller circuits 401, 401' has failed. Thus, it is quite clear that Dewey does not teach or suggest that the single dump link 426 and the RAMs 422 and 424 are used so as to obtain data which may be stored in the storage device of another cluster in response to a write request requiring updating as in the present invention.

Therefore, Dewey fails to teach or suggest that <u>when a first disk controller receives from a host computer a write request, which request updating data for updating data stored in disk drives of a second disk controller, the first disk controller</u>

checks whether the updating data is stored in the cache memory of the second disk controller, and if the updating data is not stored in the cache memory of the second disk controller, the first disk controller sends the write request to the second disk controller via the communication path as recited in the claims.

Further, Dewey fails to teach or suggest that the second disk controller, in response to the write request from the first disk controller, reads the updating data from the disk drives of the second cluster to the cache memory of the second disk controller via the disk interface of the second disk controller and updates the data based on the write request as recited in the claims.

Even beyond the above described differences between the features of the present invention as recited in the claims and Dewey it is also clear that Dewey fails to teach or suggest the use of plural storage devices and disk controllers in a plurality of clusters as in the present invention. Dewey simply teaches that plural controller circuits 401, 401' are provided with each being connected to the very same disk drives 404, 406 and 408 contrary to the present invention. The claims of the present application specifically recite that each cluster has its own disk controller and disk drives different from that taught by Dewey.

Further, Dewey does not teach or suggest that each of the clusters includes a cache memory which is used for storing data for updating, said data having been read from the disk drives as in the present invention. In the Office Action the Examiner alleges that the RAMs 422 and 424 of each controller circuit 401, 401' is equivalent to the cache memory of the present invention. However, the RAMs 422 and 424 as taught by Dewey are simply used for buffering data that may need to be

transferred, for example, from a failed controller circuit 401 to an operating controller circuit 401' via the single dump link 426. Thus, the RAMs 422 and 424 as taught by Dewey are not equivalent to the cache memory as recited in the claims.

Therefore, as is quite clear from the above, the features of the present invention as now more clearly in the claims are not taught or suggested by Dewey whether taken individually or in combination with any of the other references of record.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference utilized in the rejection of claims 1-18.

In view of the foregoing amendments and remarks, Applicants submit that claims 19-23 are in condition for allowance. Accordingly, early allowance of claims 19-23 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (520.39648X00).

Respectfully submitted,

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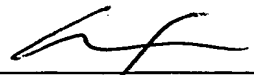

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